We Claim:

1. A method for operating a semiconductor memory, which comprises:

sharing a data read access and a data write access between a first memory bank and a second memory bank;

combining a partial data stream obtained from an output of the first memory bank and a partial data stream obtained from an output of the second memory bank to form a data stream with a doubled frequency;

operating the first memory bank with a clock being shifted by half of a clock pulse with respect to a clock of the second memory bank;

deriving the clock of the first memory bank from a falling edge of an external clock signal during the read access and from a rising edge of the external clock signal during a write access; and

deriving the clock of the second memory bank from the rising edge of the external clock signal during the read access and from the falling edge of the external clock signal during the write access.

2. A semiconductor memory, comprising:

a first memory bank having an output for providing a partial data stream;

a second memory bank having an output for providing a partial data stream;

a clock control unit; and

a multiplexer apparatus for sharing a data read access and a data write access between said first memory bank and said second memory bank;

said partial data stream provided by said output of said first memory bank and said partial data stream provided by said output of said second memory bank being combined to form a data stream with a doubled frequency;

said clock control unit configured for obtaining an external clock signal;

said clock control unit deriving a clock for operating said first memory bank from a falling edge of said external clock signal during a read access and from a rising edge of said external clock signal during a write access;

said clock control unit deriving a clock for operating said second memory bank from said rising edge of said external clock signal during said read access and from said falling edge of said external clock signal during said write access; and

said clock for operating said first memory bank being shifted by half a clock pulse with respect to said clock for operating said second memory bank.

3. The semiconductor memory according to claim 2, wherein:

said multiplexer apparatus includes a first multiplexer for, during said read access, combining said partial data stream provided by said output of said first memory bank and said partial data stream provided by said output of said second memory bank to form said data stream with said doubled frequency;

said multiplexer apparatus includes a second multiplexer for, during said write access, dividing an input data stream into a partial data stream to be written into said first memory bank and a partial data stream to be written into said second data bank; and said first multiplexer and said second multiplexer are clocked by said clock for operating said first memory bank and by said clock for operating said second memory bank.